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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,861	10/29/2003	Hiroshi Makamura	244682US2S	5717

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EXAMINER	
NGUYEN, NAM THANH	
ART UNIT	**PAPER NUMBER**
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,861	MAKAMURA ET AL.	
	Examiner	Art Unit	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-22* is/are rejected.

7)☒ Claim(s) *9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 12/12/06 has been entered.

Claim 14 has been cancelled.

Claims 15-22 are newly added.

Claims 1-13 and 15-22 are pending tin the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-8,12-13 and 15-22 are rejected under 35 U.S.C. 102(e) as being anticipated by the admitted prior art.

Regarding claims 1 and 15, The admitted prior art (figures 1 and 2, and pages 2-9 of the instant application) disclose a plurality of memory cell arrays (Array 0, Array1, Array 2, Array 3 of the instant application) having of a plurality of memory cells or memory cell units (the cell array is inherently includes a plurality of memory cells and units or a group of cells) which includes a plurality of memory cells, arranged in a

matrix, wherein the plurality of memory cell arrays (Array 0, Array1) are located independently of each other (as shown in the admitted prior art in figure 2 of the instant application) and have a plurality of cell array groups each of which have two or more memory cell arrays, (in the instant case, the upper Array 0 and the lower Array0 would be one cell array group and the upper Array1 and the lower array 1 would be another cell array group) a first Pass/Fail signal (see page 5, lines 11-15 of the instant application) indicative of success or failure of an operation is outputted in accordance with each cell array group (see page 5, lines 25-26 and page 6, lines 1-15 of the instant application) and the semiconductor memory device is a memory chip (see fig. 2) including all of the plurality of memory cell array groups

Regarding claims 2-3 and 16-17, a parallel operation with respect to memory cells in two or more of the plurality of cell array groups (see page 9, lines 1-4).

Regarding claims 4 and 18, the operation recited in page 5, lines 10-15 is a program operation or an erasing operation.

Regarding claims 5 and 19, the first Pass/Fail signal is a Pass/Fail signal indicating whether the operation has attained success with respect to all of selected memory cells or not (see page 5, lines 27-28 and page)

Regarding claims 6 and 20, a second Pass/Fail signal of an entire chip (EEPROM chip) is also outputted when the first Pass/Fail signal is outputted (see page 6).

Regarding claims 7 and 21, a Pass/Fail signal indicating whether the operation has attained success with respect to one memory cell array selected from the two or more memory cell arrays in each of the cell array groups or not (see page 8, lines 7-11 and table 1 in page 6 and table 2 in page 7).

Regarding claim 8, the first Pass/Fail signal is outputted after a first command is inputted (see page 8, lines 7-21 and table 1 in page 6 and table 2 in page 7).

Regarding claim 12-13 and 22, line 11 in page 5 discloses the memory is EEPROM and the memory cell unit is a NAND cell type.

Allowable Subject Matter

4. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to:

"a third Pass/Fail signal which is different from the first Pass/Fail signal is outputted after a second command is inputted" as claimed in the dependent claim 9; or

"a forth Pass/Fail signal is outputted with respect to each of the cell arrays included in an entire chip after a third command is input" as claimed in the dependent claim 10.

Response to Response

5. The applicant argues that the upper array 0 and lower array 0 are found on different chips and claims 1 and 15 recite that the semiconductor memory device comprises a memory chip including all of the plurality of memory cell array groups. The Examiner disagrees. Fig. 2 (PRIOR ART) clearly shows a 1Gbit (first generation) chip that is considered as a single memory chip.

Therefore, the applicant arguments are not persuasive for the reasons set forth above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

5. The following prior art, which is considered pertinent to applicant's disclosure although not relied upon, includes:

Hosono et al. (US 2003/0214853) or Sakui et al. US. Pat no. 6,031,760) or Chen et al. Pub. No.: US 2004/0145952) disclose EEPROM cell array with pass/fail function similar to that of the present application, but fail to disclose the claimed limitations as described above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T. Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam T Nguyen
Examiner
Art Unit 2824

1/10/07

SON DINH
PRIMARY PATENT EXAMINER